

FIG. 1

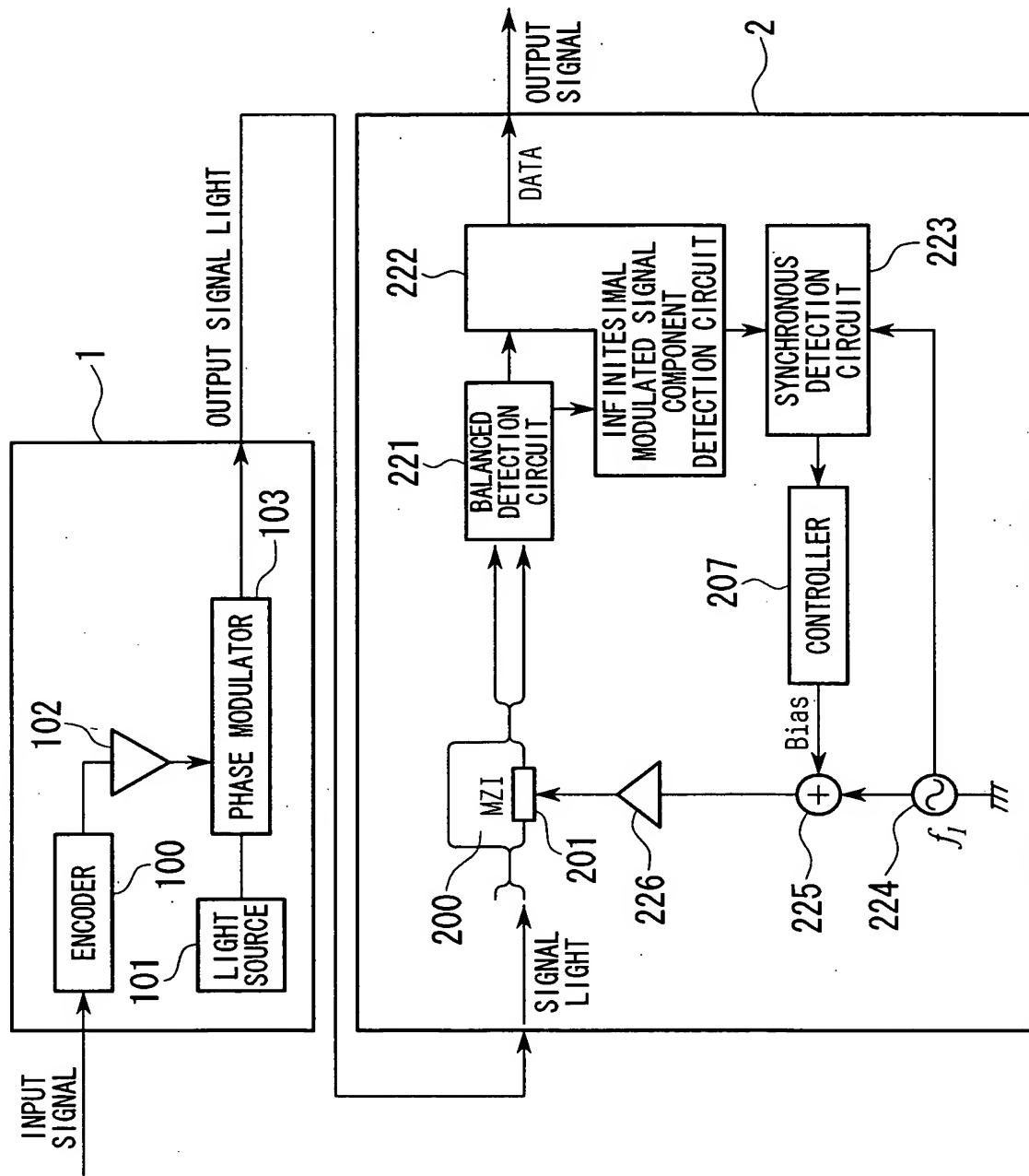


FIG. 2

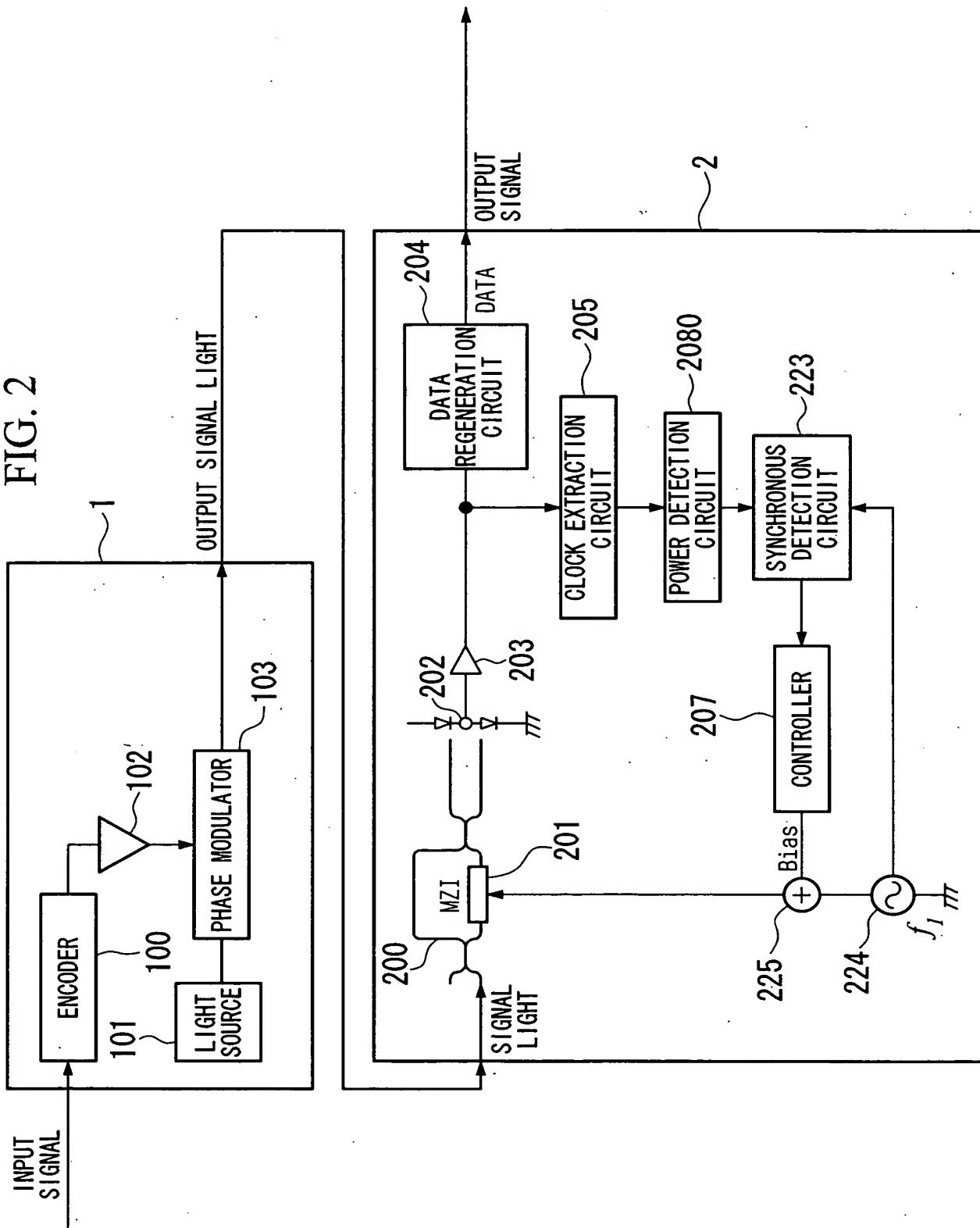
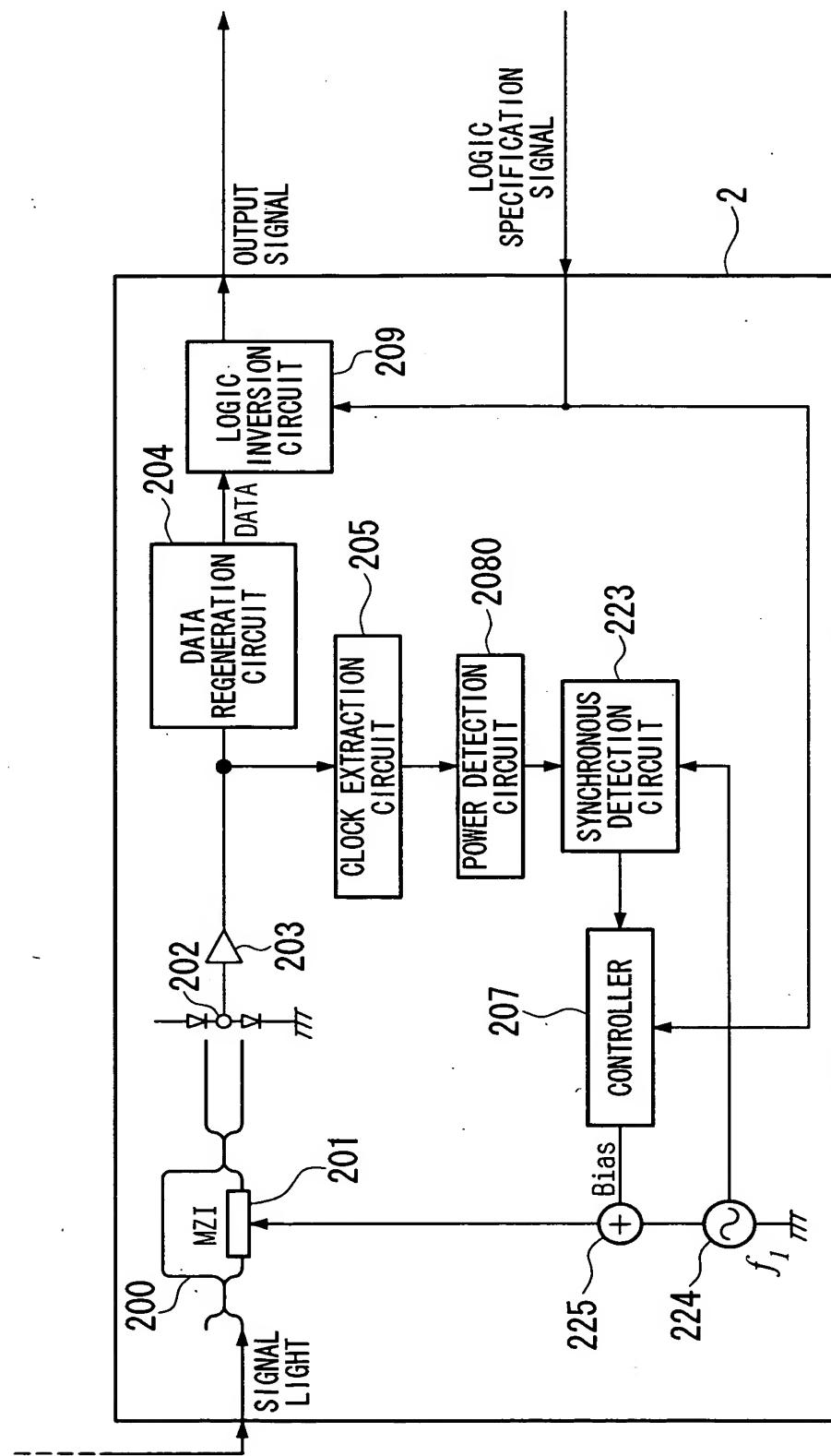


FIG. 3



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FIG. 4

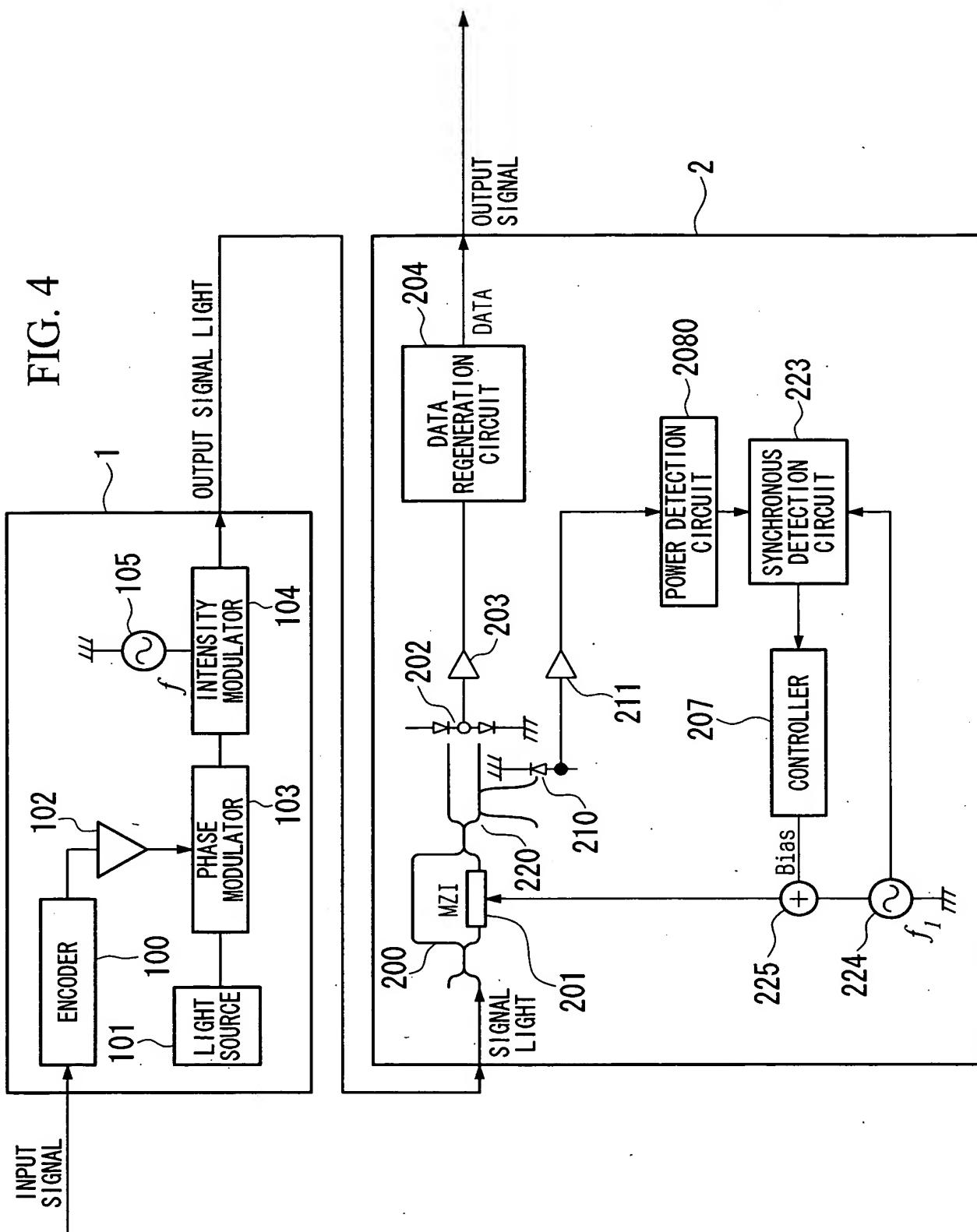
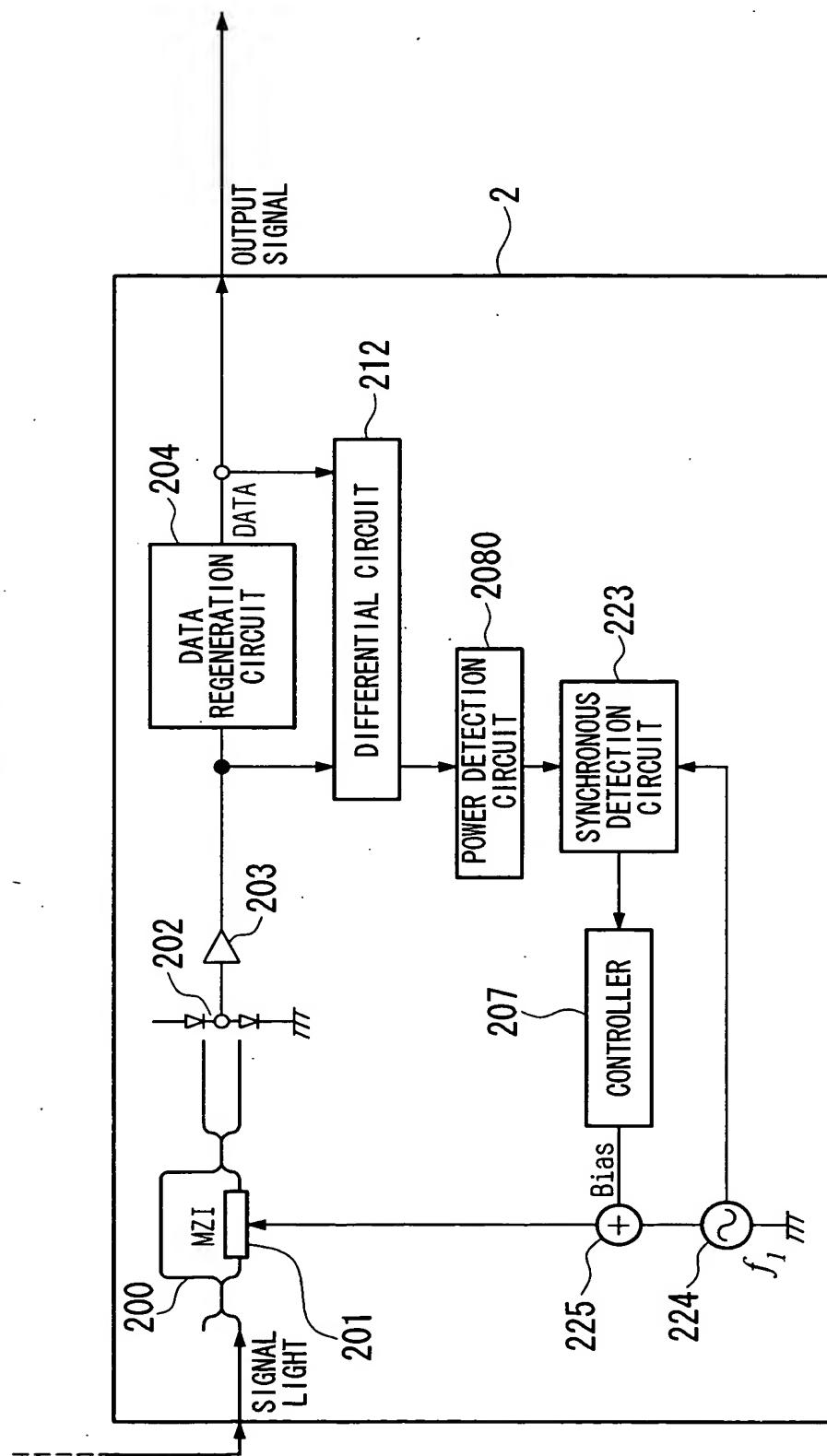


FIG. 5



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FIG. 6

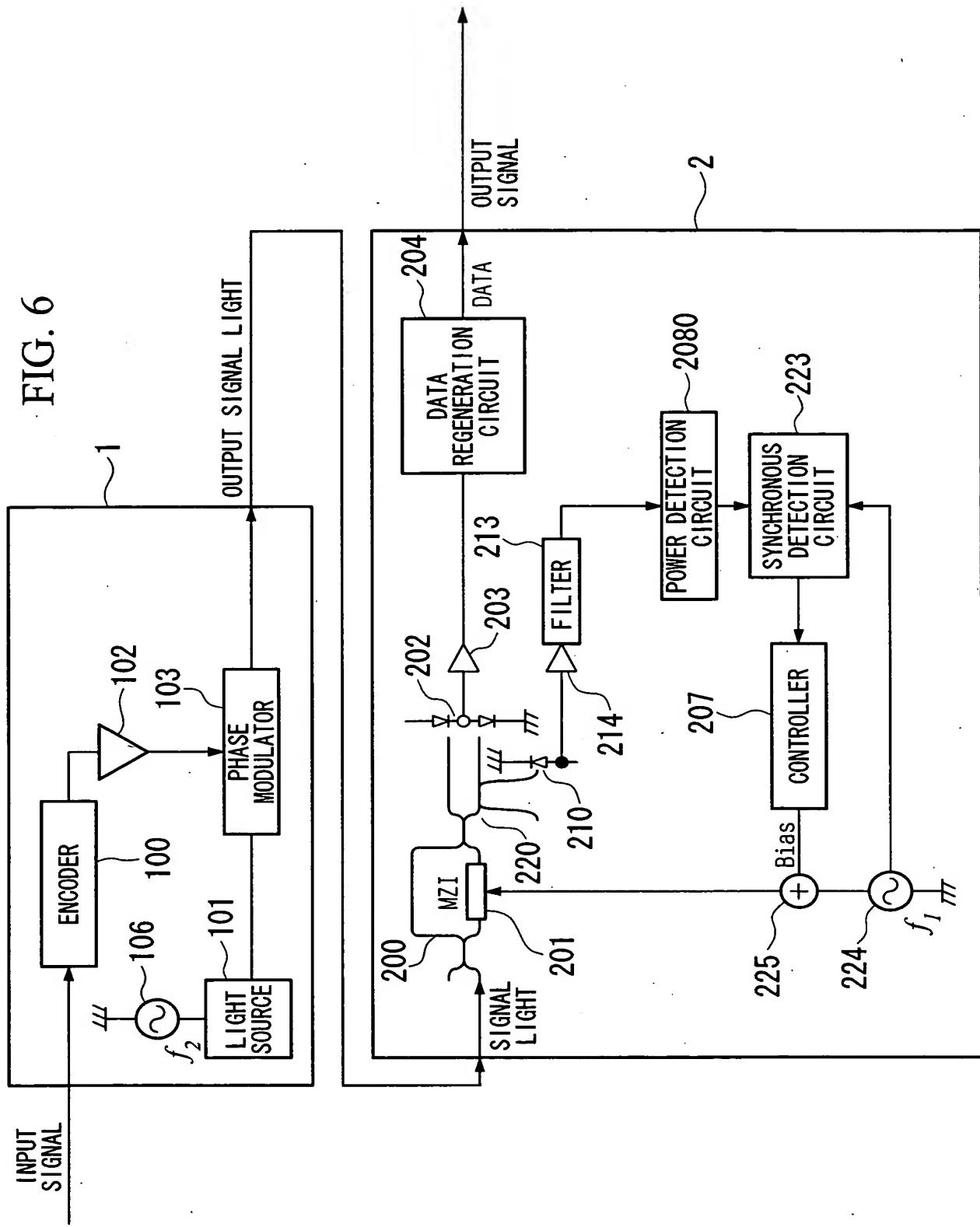
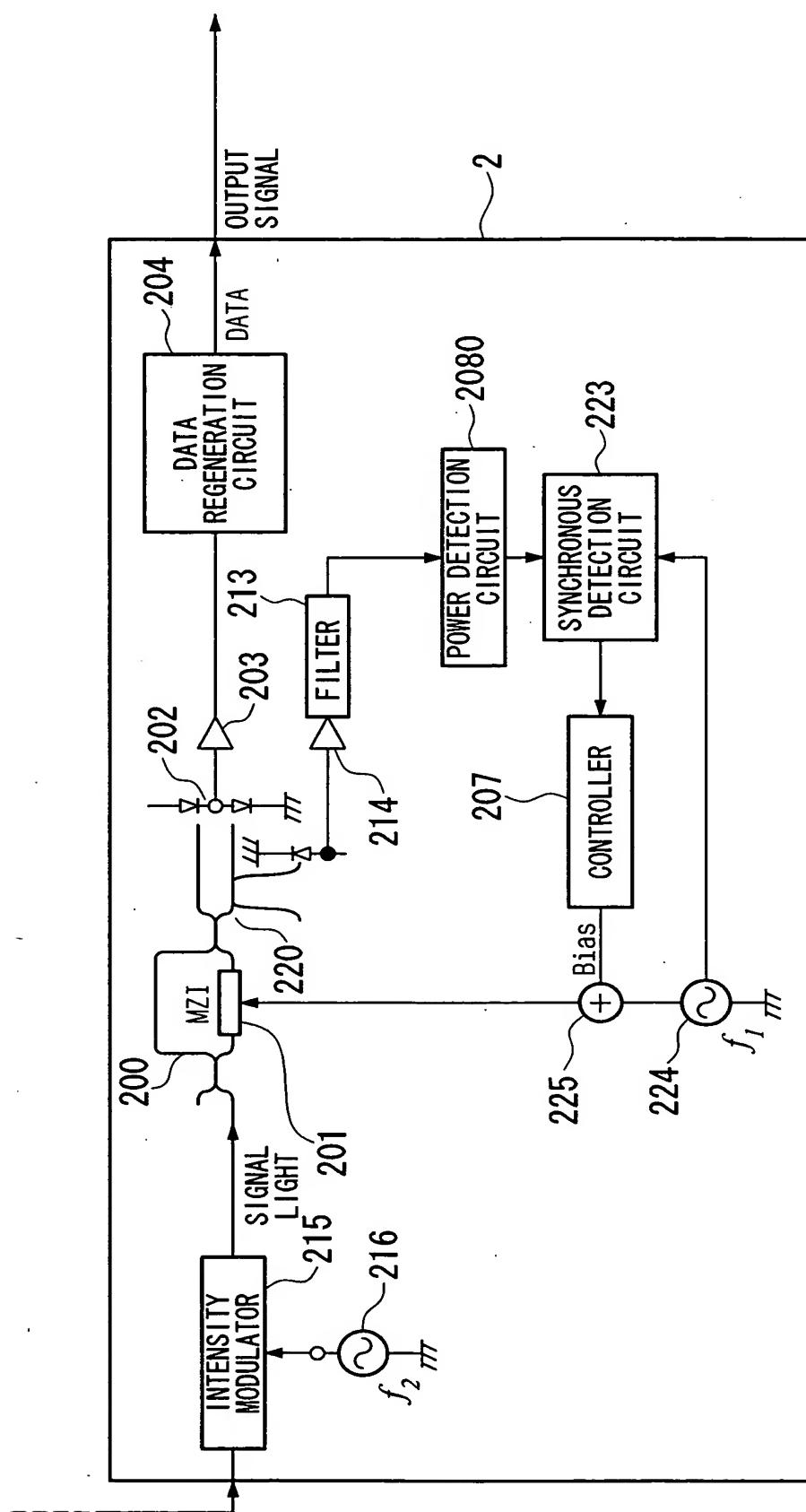


FIG. 7



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FIG. 8

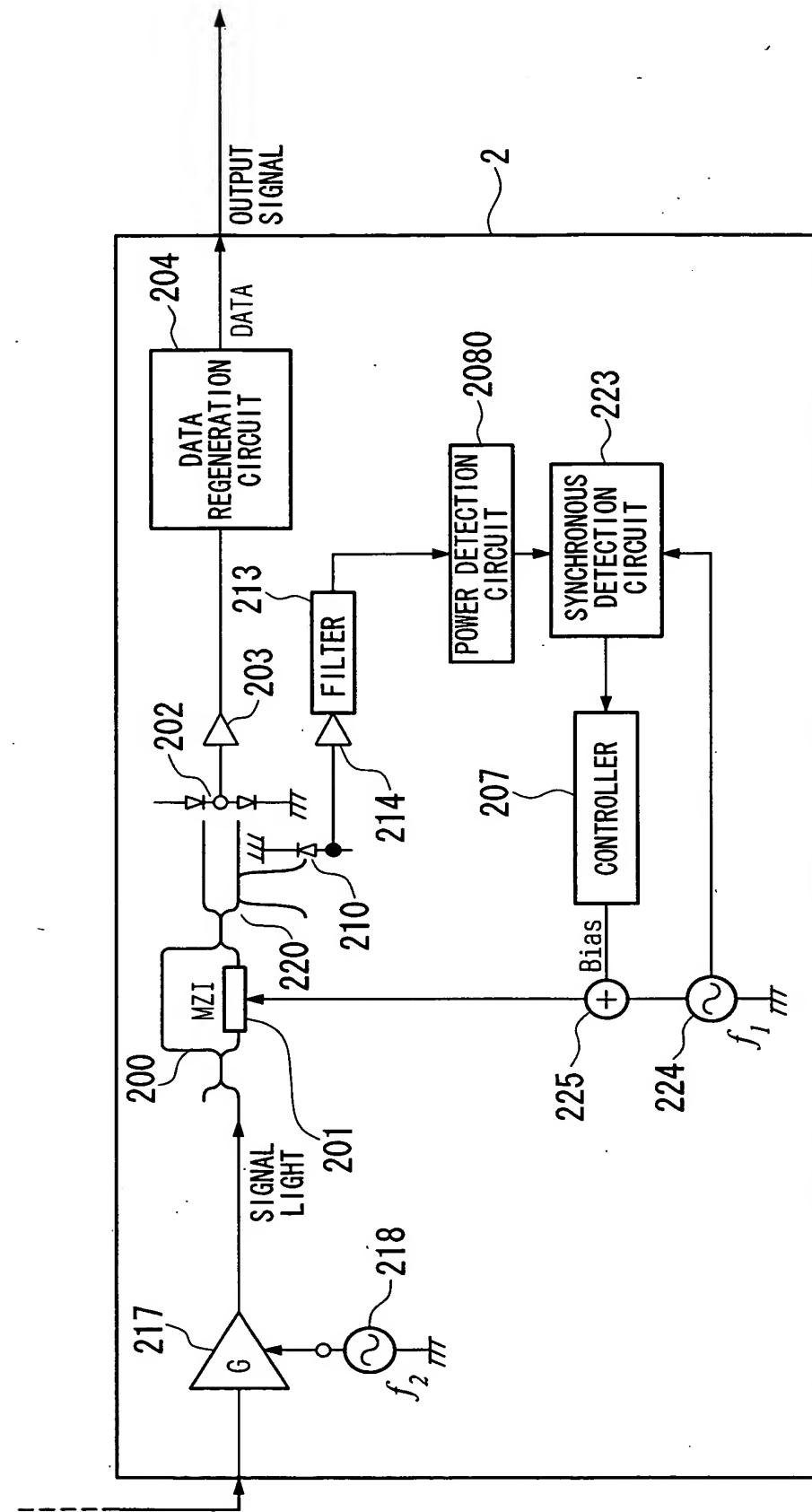
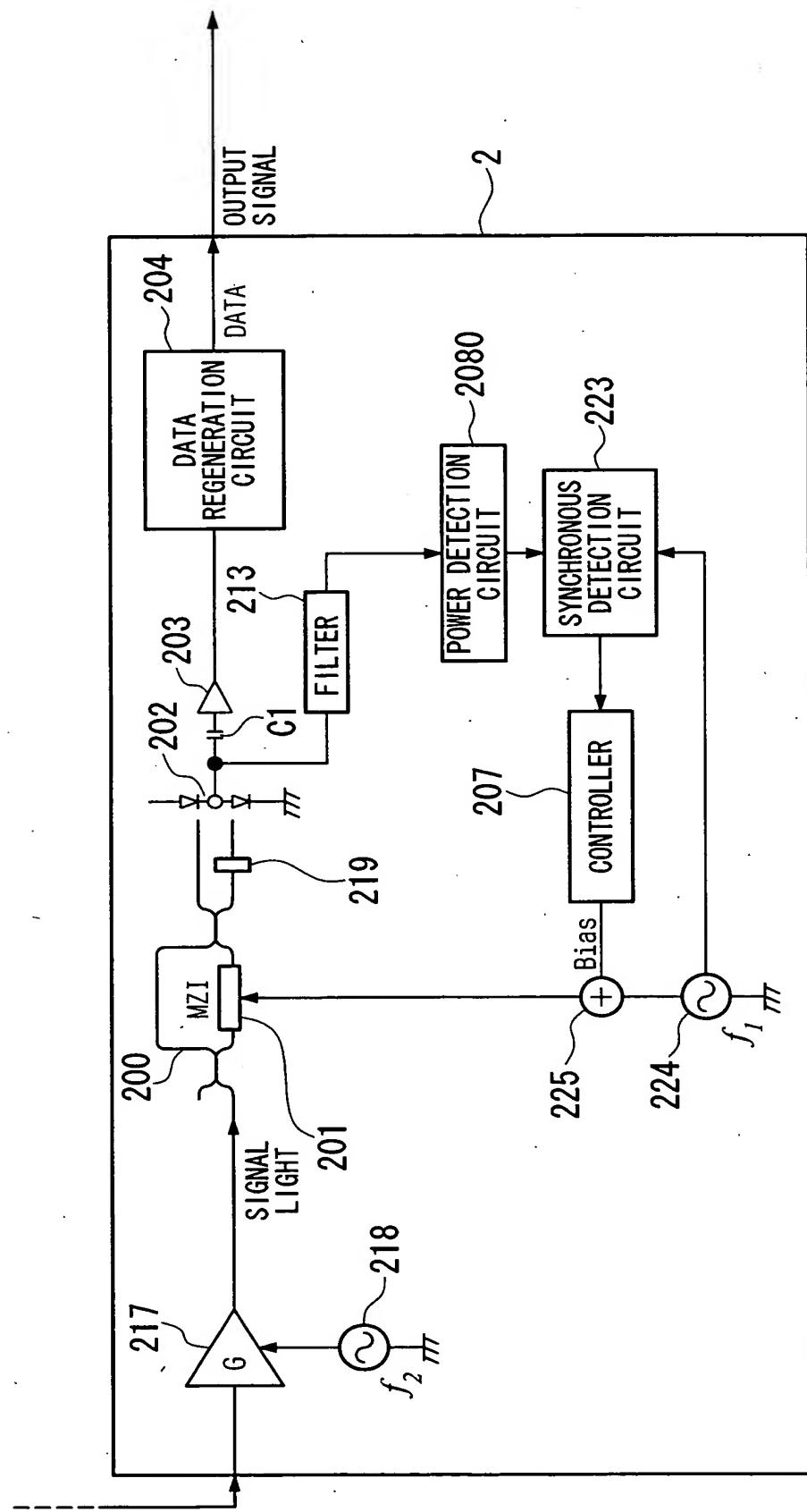
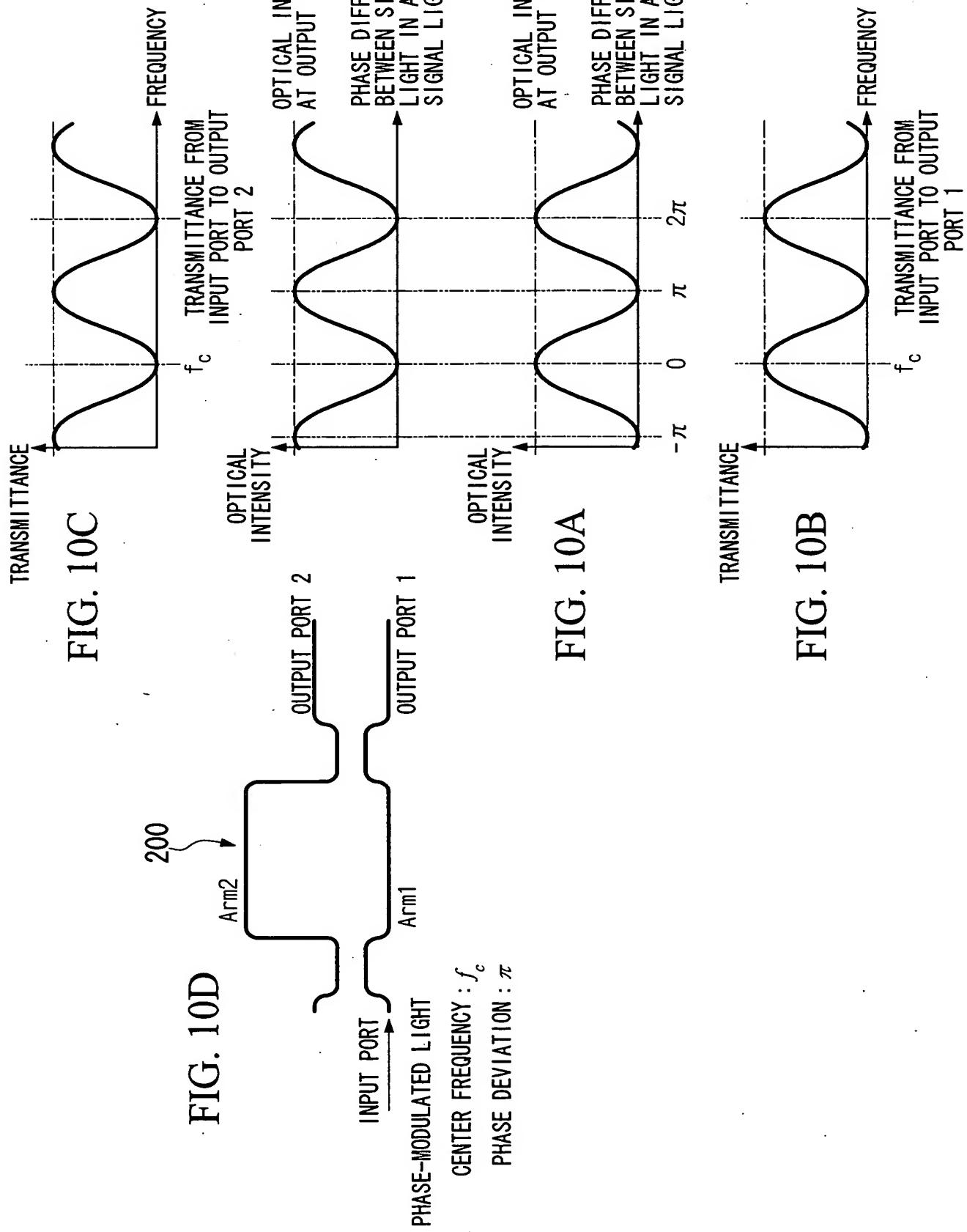


FIG. 9



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FIG. 11

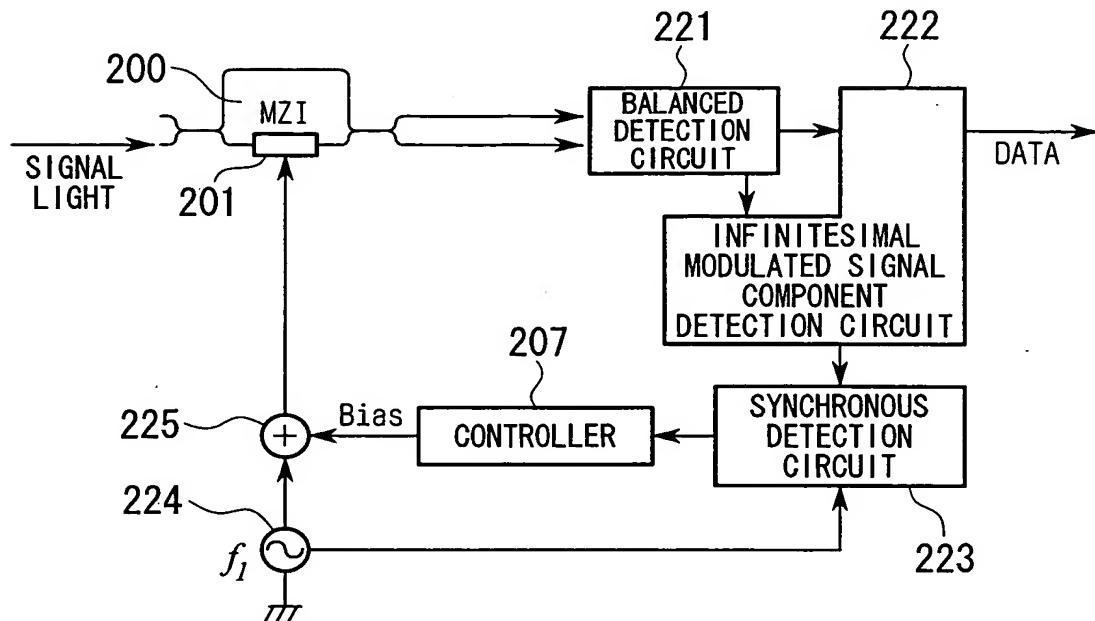


FIG. 12

OUTPUT VOLTAGE OF BALANCED
DETECTION CIRCUIT

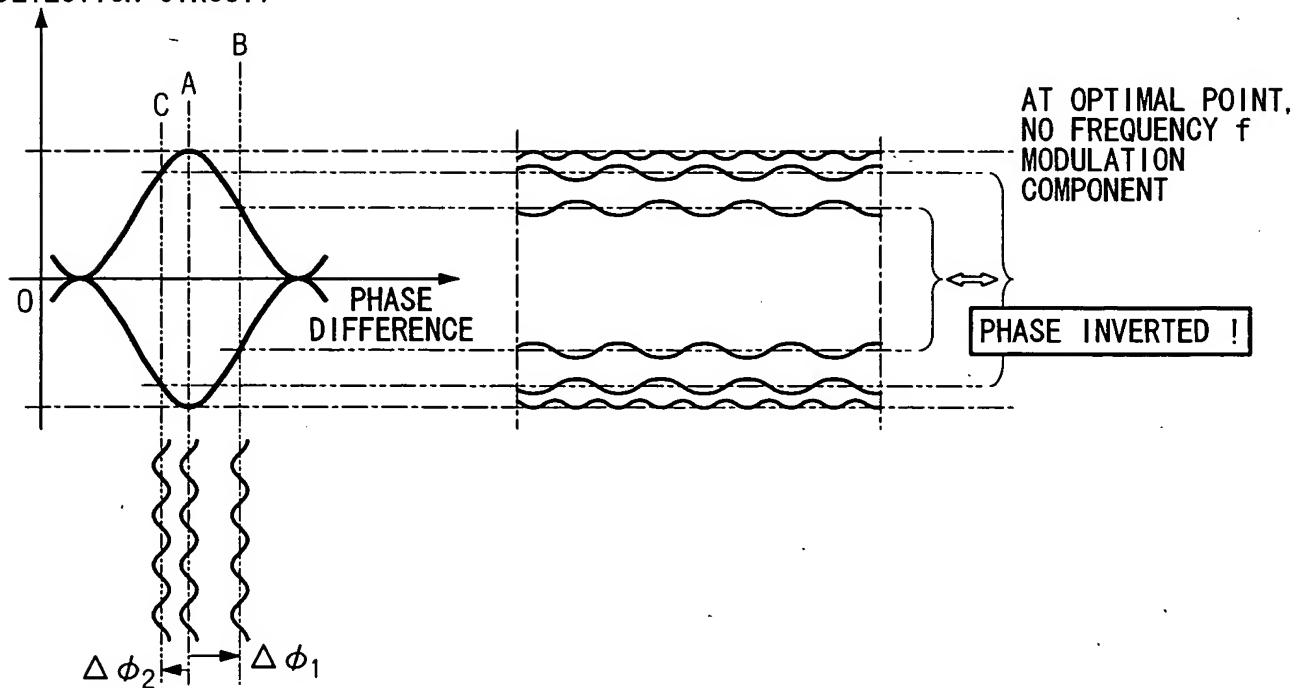


FIG. 13

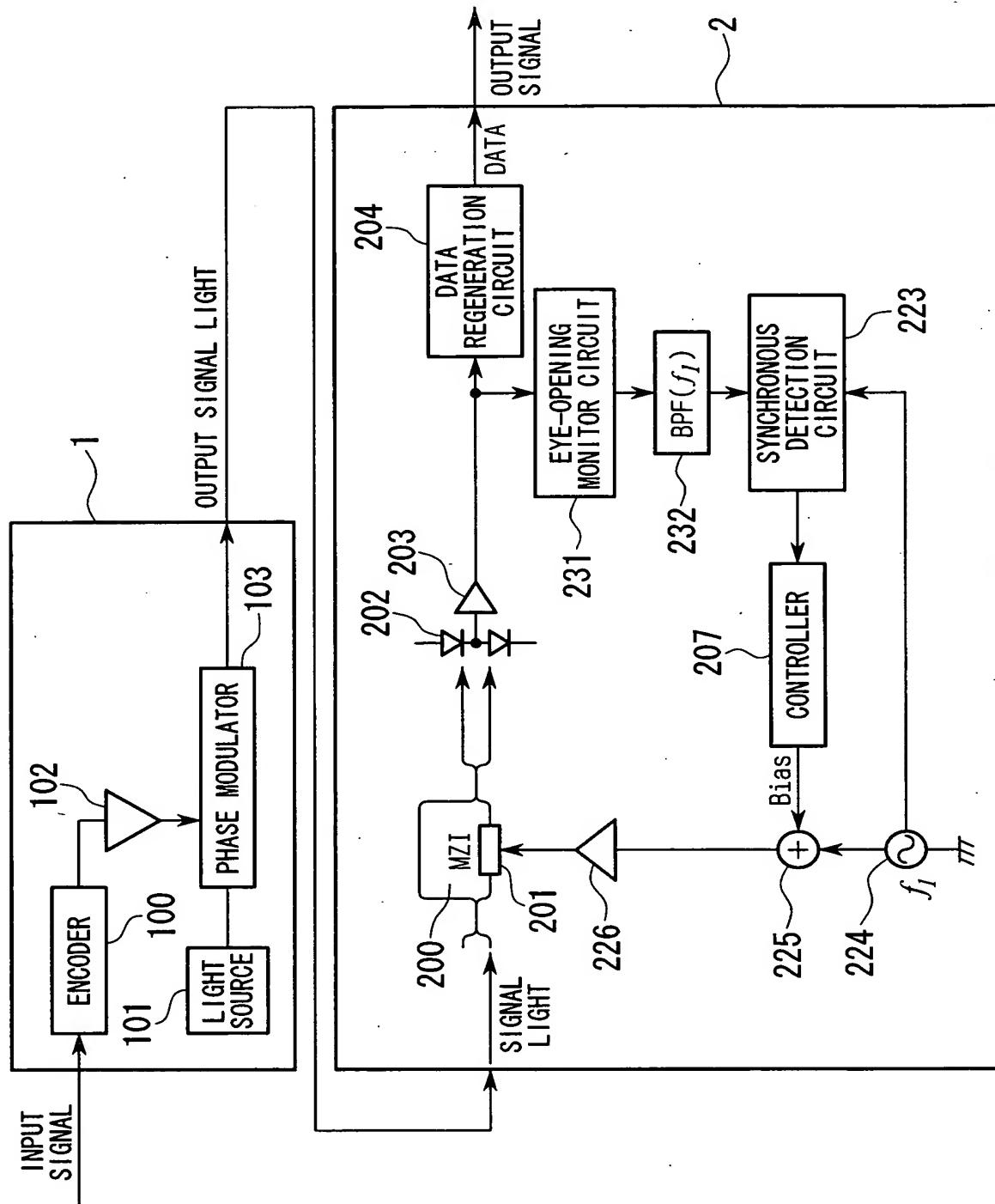
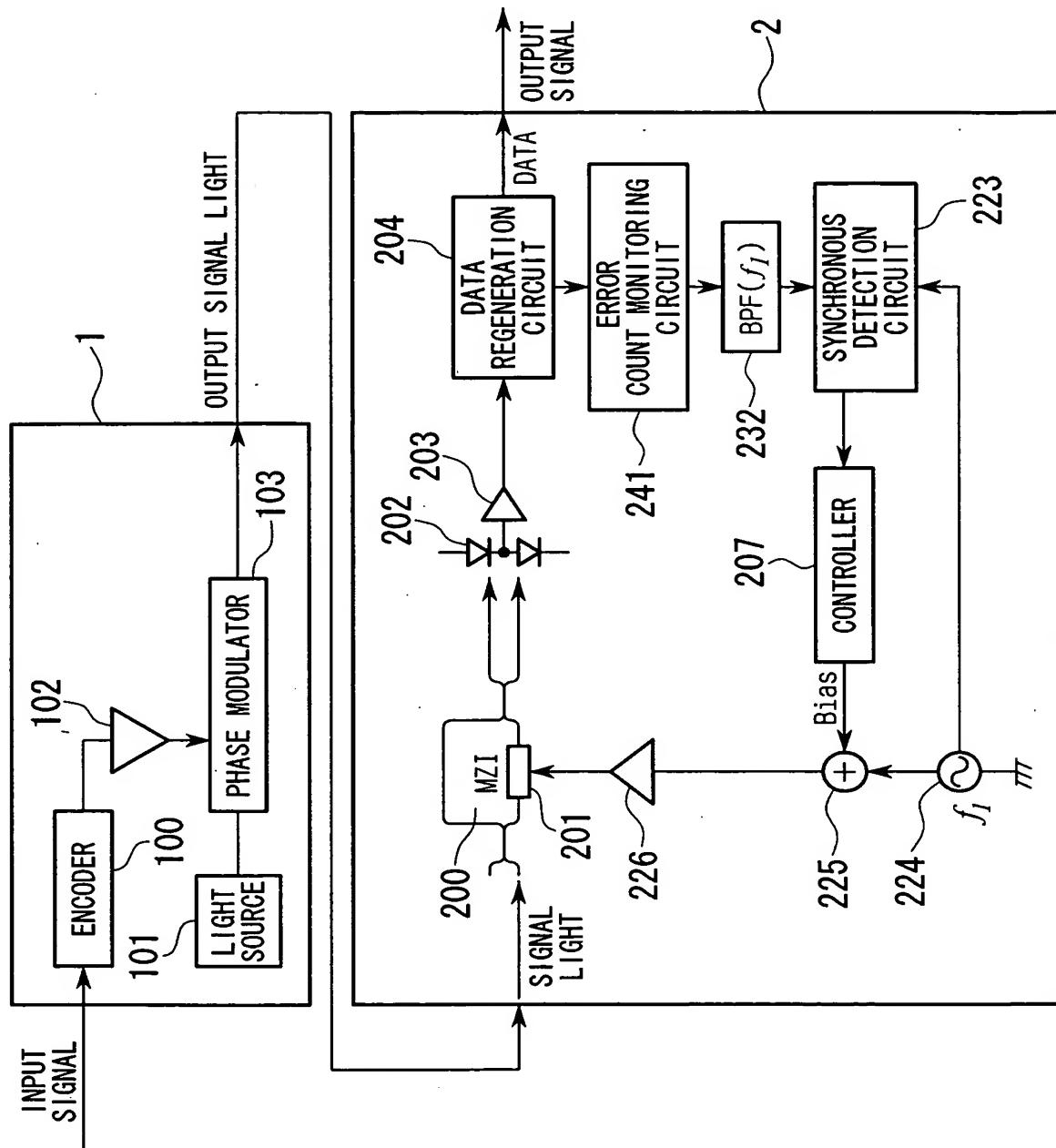


FIG. 14



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FIG. 15

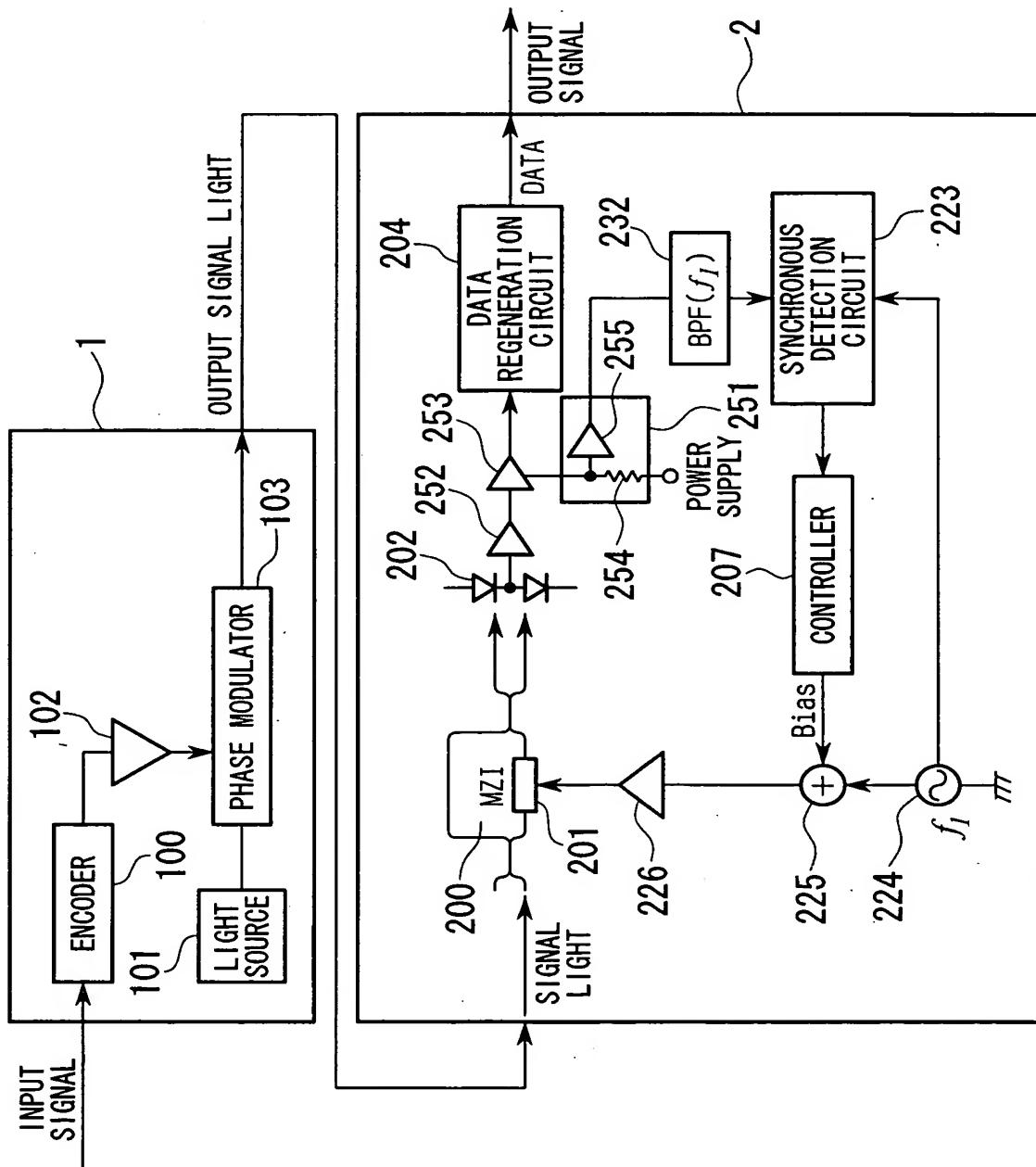
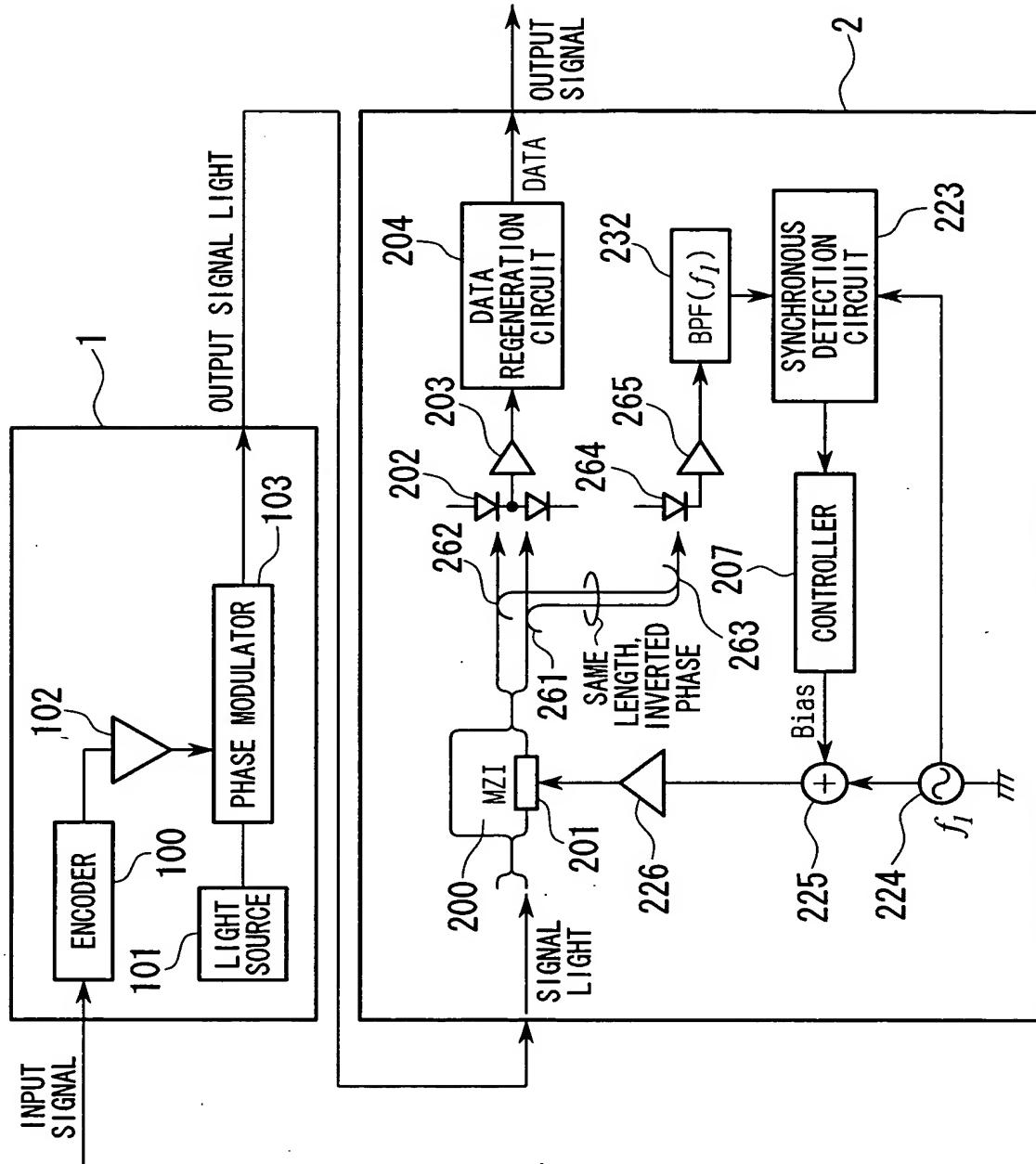


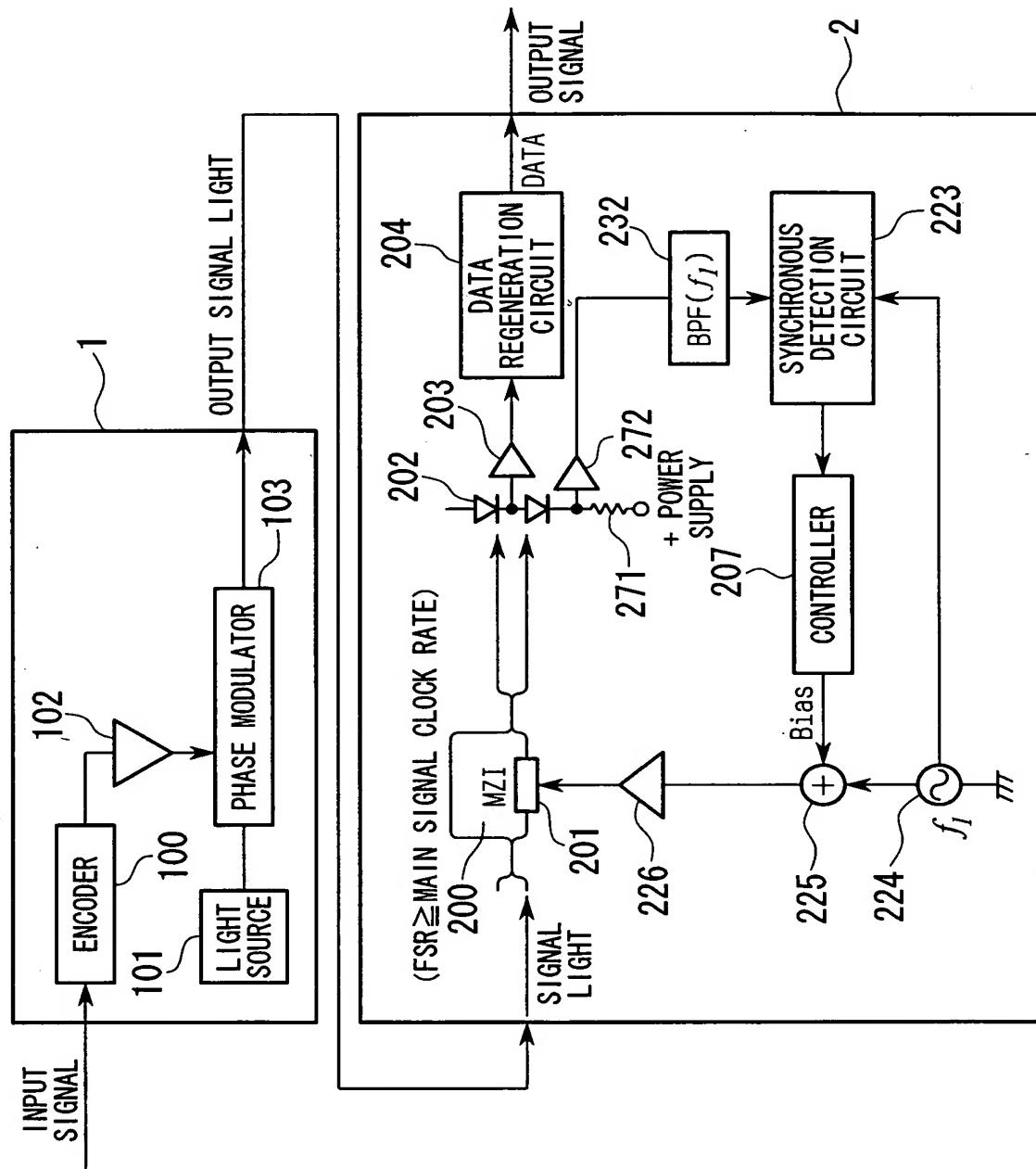
FIG. 16



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FIG. 17



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FIG. 18

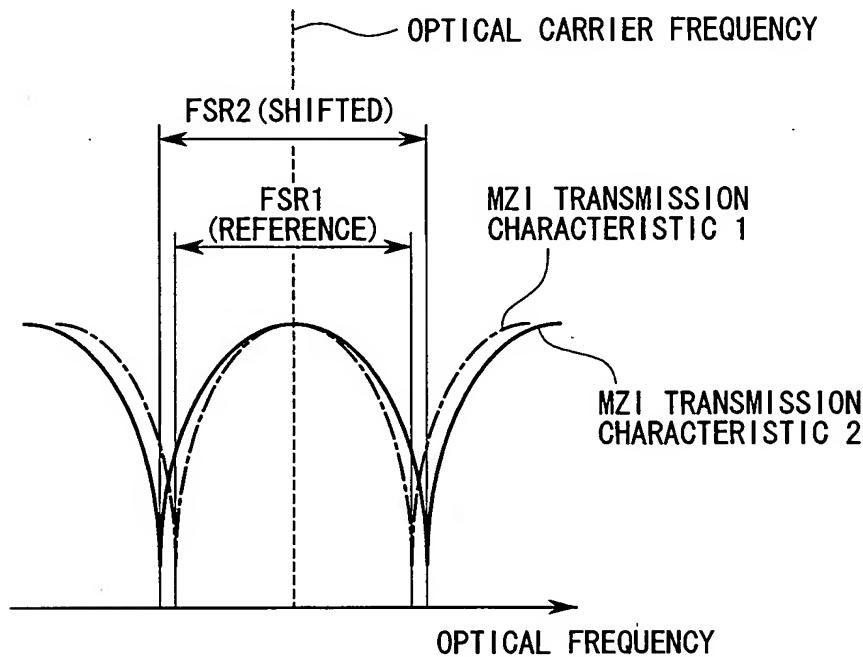
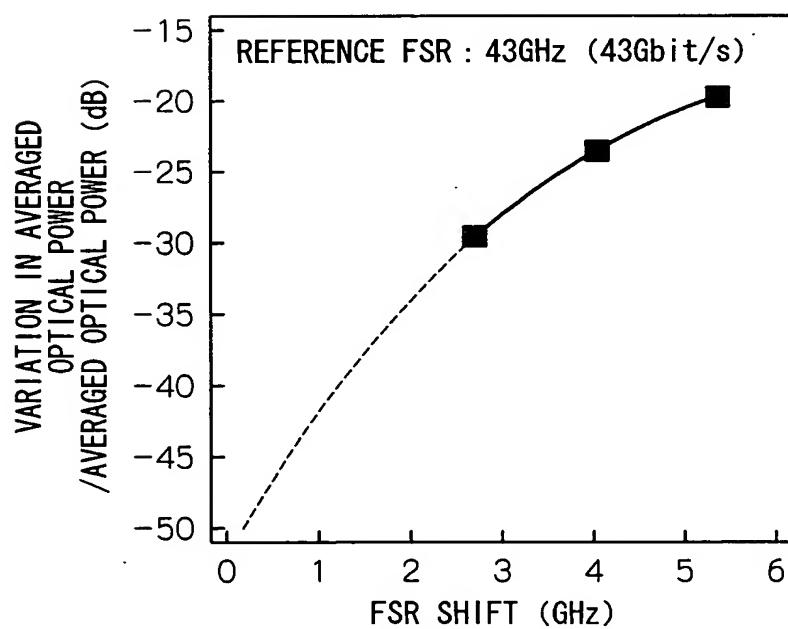


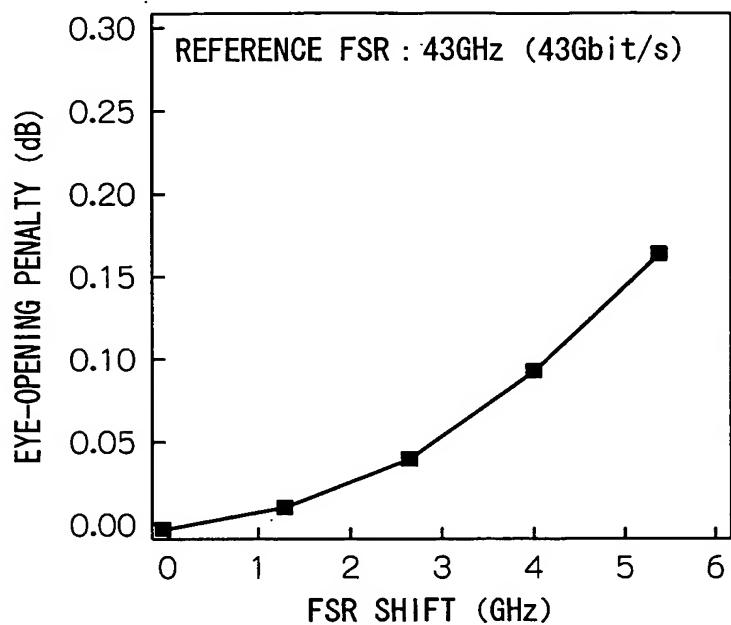
FIG. 19



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FIG. 20



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FIG. 21

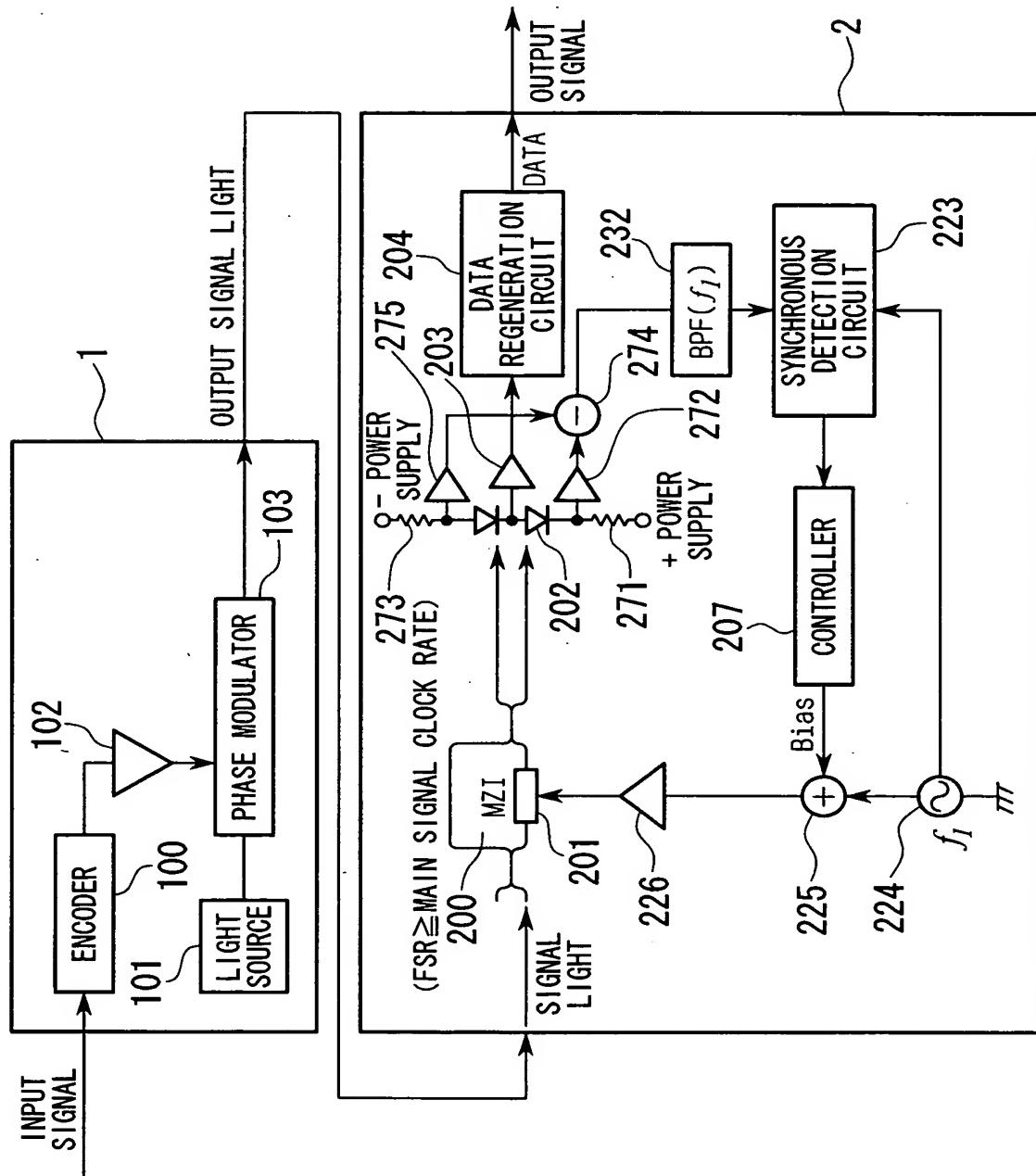


FIG. 22

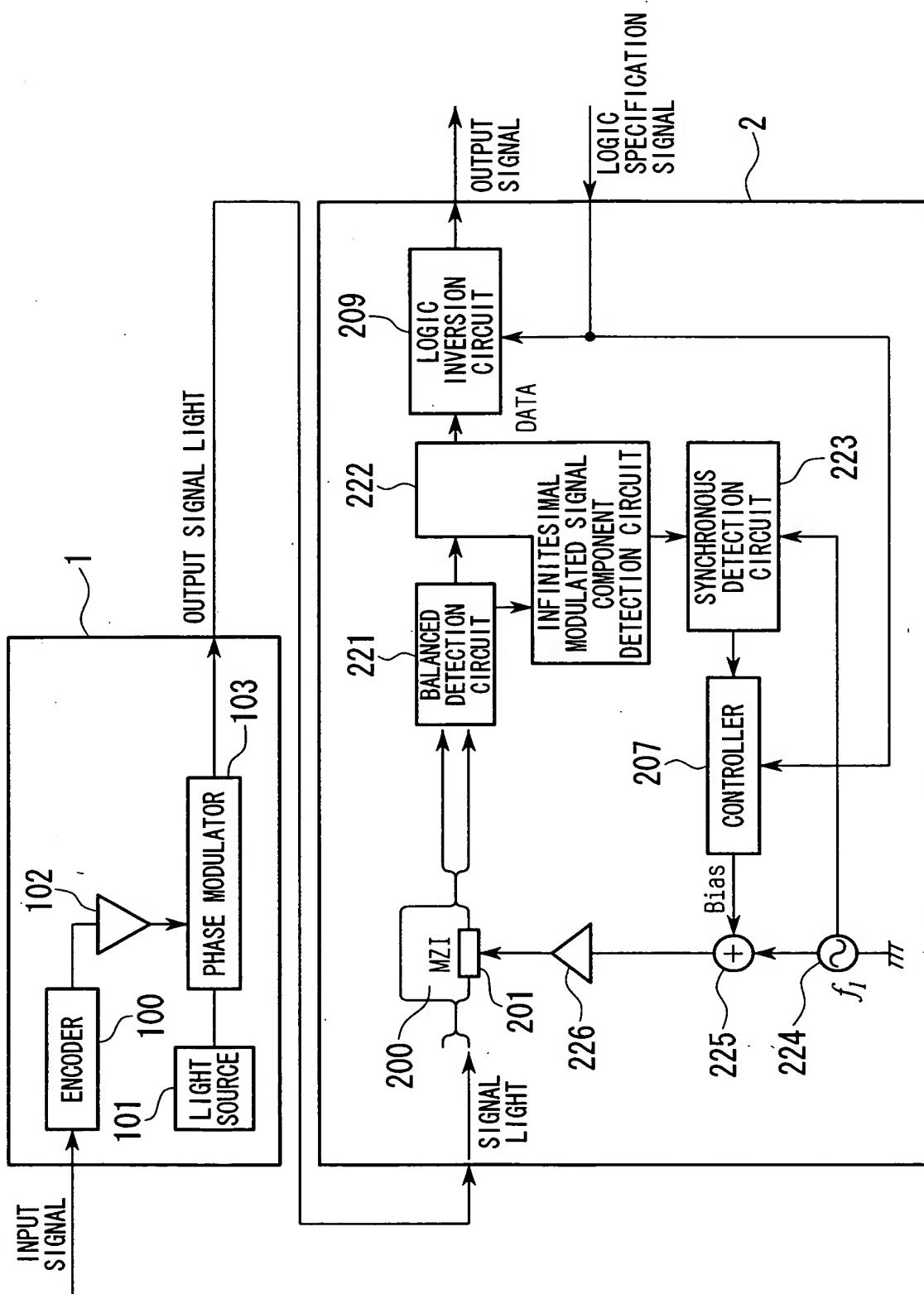
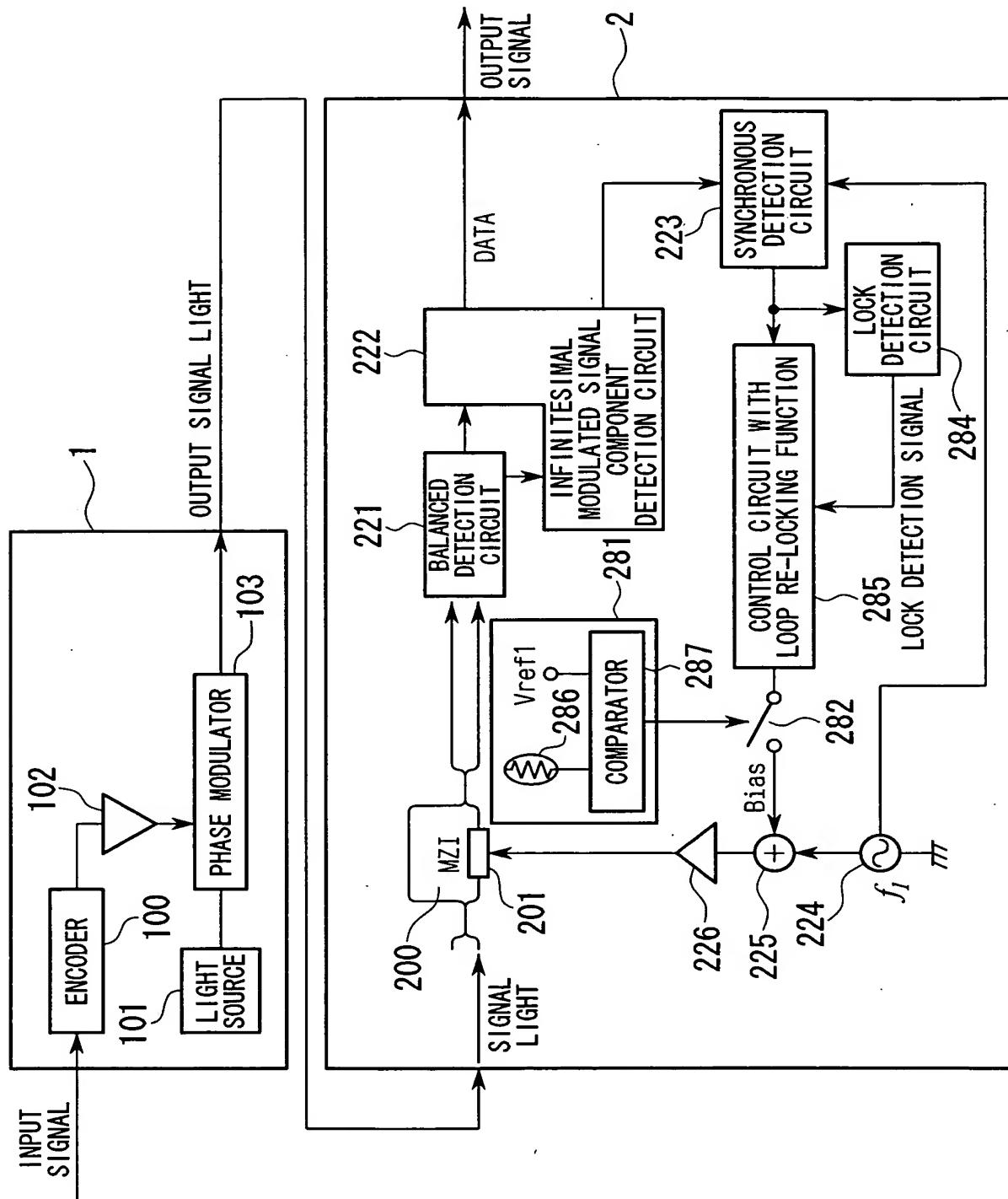


FIG. 23



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FIG. 24

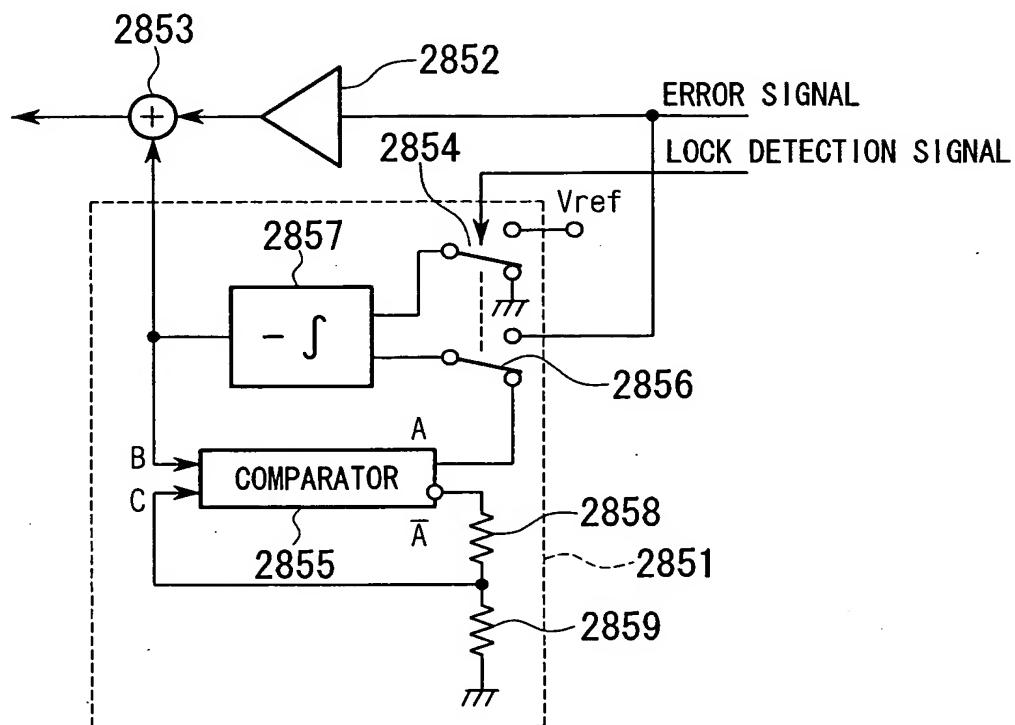
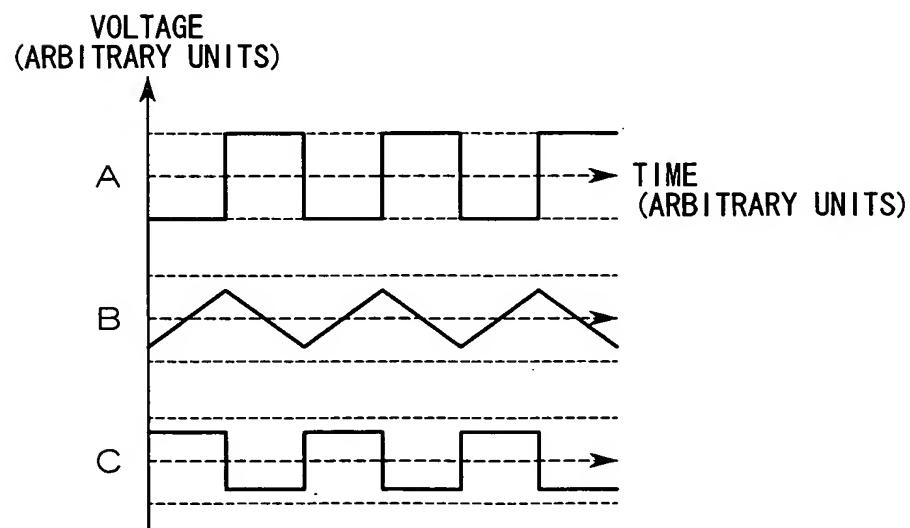


FIG. 25



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FIG. 26

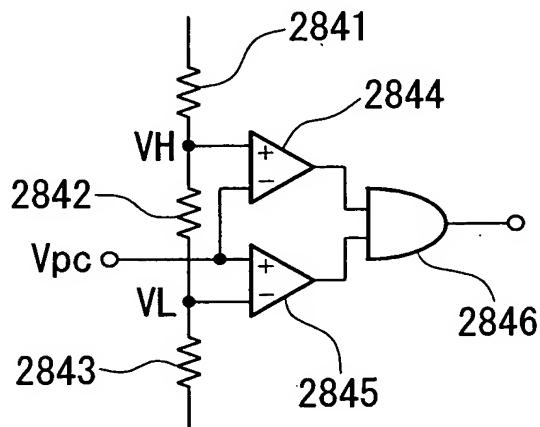
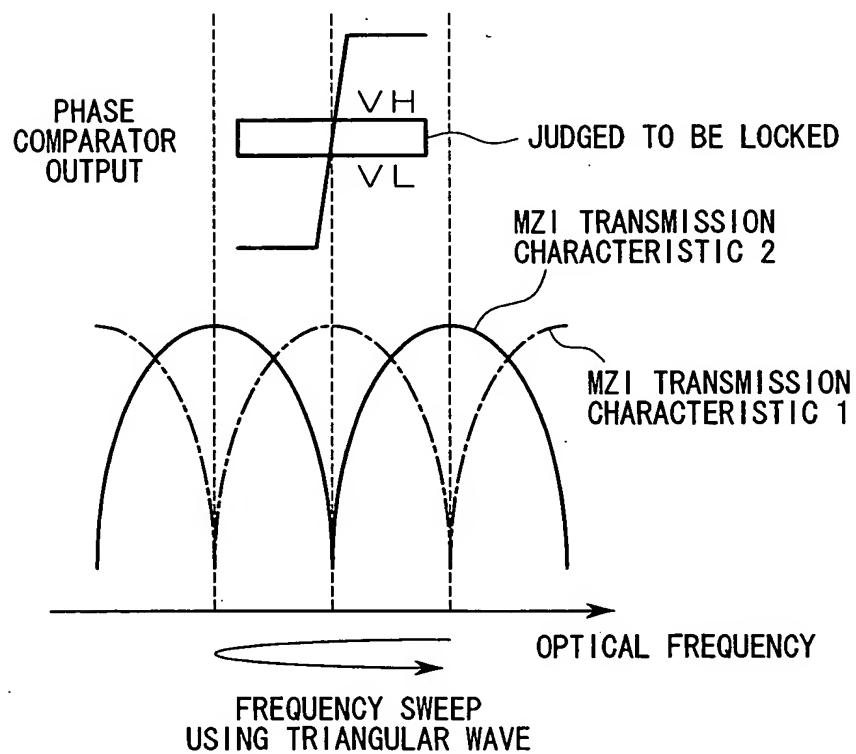


FIG. 27



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FIG. 28

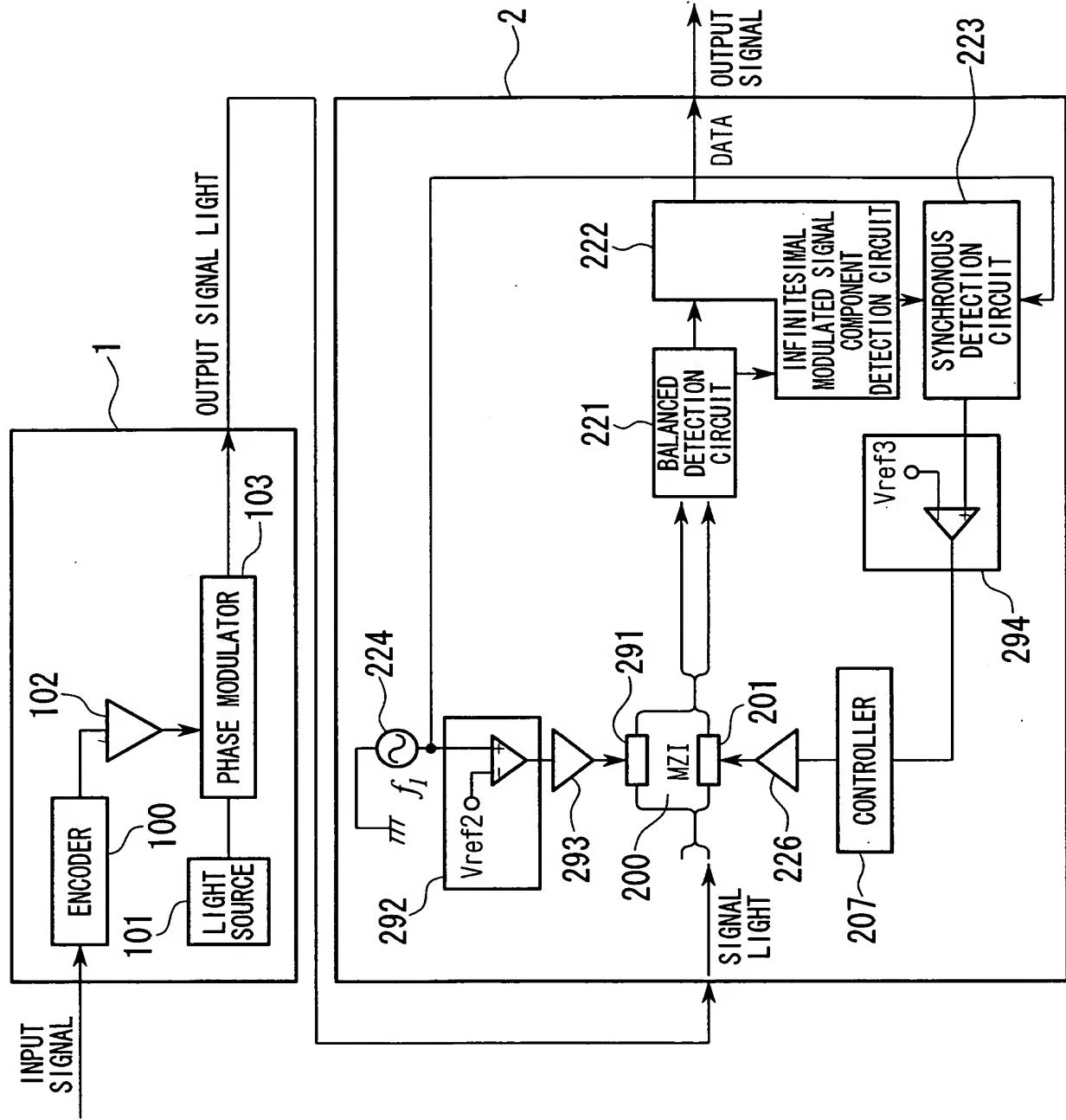


FIG. 29

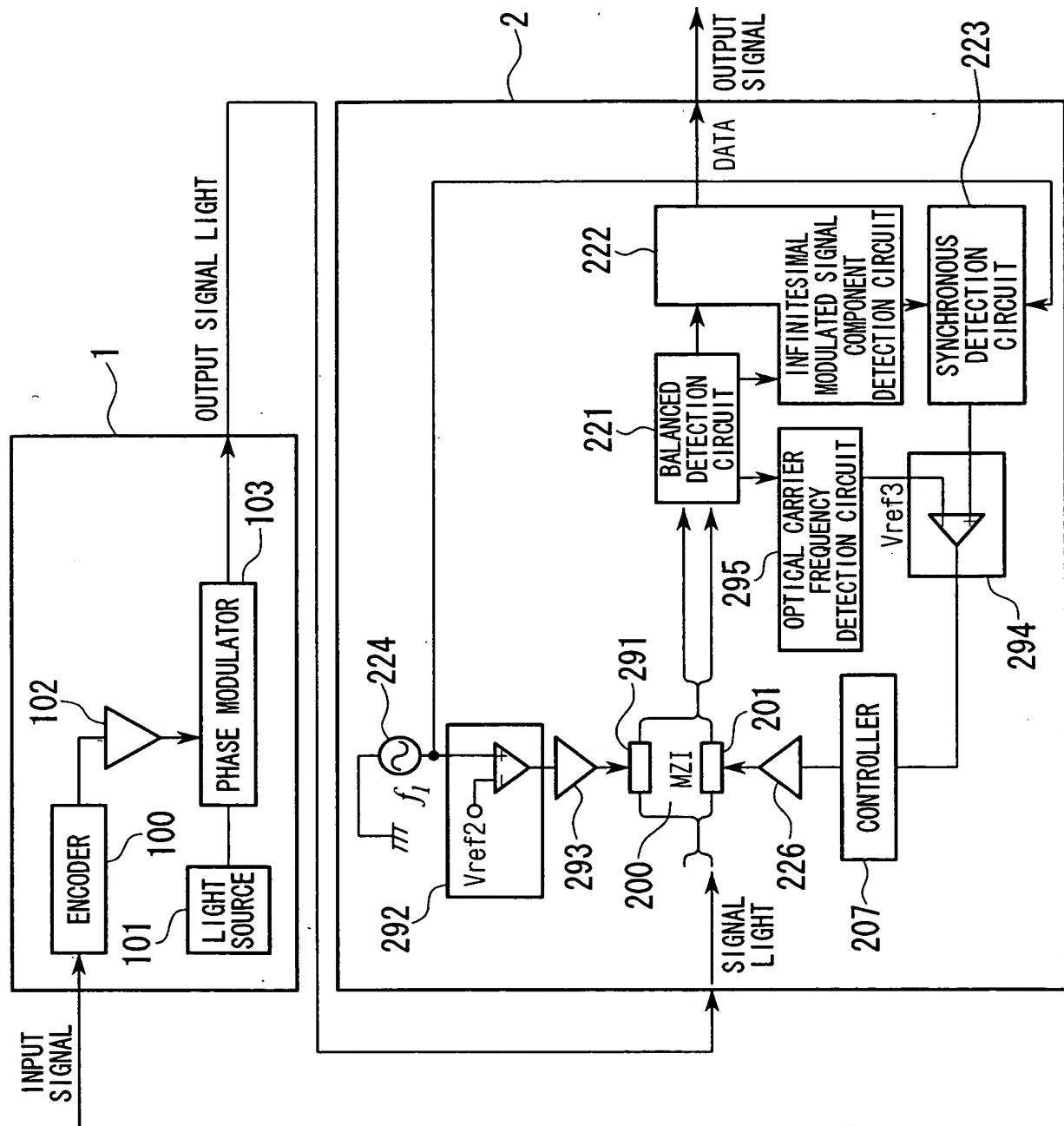


FIG. 30

